VLSI B.Tech/B.E IEEE Projects List

Front End Design(VHDL/Verilog HDL)		
S.No	**PROJECT NAME**	**IEEE YEAR**
1	EEG Signal Denoising based on Wavelet Transform	2018
2	LUT Based Multiplier for Short Word Length DSP Systems	2018
3	MROBA and MAC Unit Design for Digital Signal Processing	2018
4	Binary To Gray Code Converter Implementation Using QCA	2018
5	Flip-Flop Circuits using Quantum Dot Cellular Automata (QCA)	2018
6	A Bit-Plane Decomposition Matrix-Based VLSI for HEVC Using Integer Transform Architecture	2018
7	GALS Modeling for Communication Circuits	2018
8	Improved 64-Bit Radix-16 Booth Multiplier	2018
9	Advanced P-OCI Crossbar with PaCC Codec	2018
10	An Adaptable Deep Learning Accelerator Unit (DLAU) for FPGA	2018
11	A Novel PRPG for Low Power Applications	2017
12	A New Algorithm For Multiple Constant Multiplications With Low Power Consumption	2017
13	Design of MAC Unit For DSP Applications Using Verilog HDL	2017
14	Floating-Point Butterfly Architecture Based On Multi Operand Adders	2017
15	VLSI Architecture For Montgomery Modular Multiplication Algorithm By Using Pasta Adder	2017
16	Pre encoded Multiplier Architecture Based On NR4SD Encoding Technique For DSP Applications	2017
17	Design And Implementation Of High Speed Accelerator Using Carry Save Adder	2017

Head Office: G3, Ratna Complex, Image Hospital Lane, Beside DHFL, Ameerpet
Hyderabad - 500073, Contact: 7036987111/222/333/444
Branch Office: 2nd Floor, Datta Lord House, Behind PVP Cinemas, M.G.Road, Labbipet
Vijayawada - 520002, Contact: 7036987666

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18	VLSI Design Of A Novel Pre Encoding Multiplier Using DADDA Multiplier	2017
19	Fault Tolerant Parallel Filters design For Communication Applications	2017
20	A Transparent Test Technique For Detection Of Faults In FIFO Buffers Of NOC Routers	2017
21	Design Of 16-Bit Multiplier Using Modified Gate Diffusion Input Logic	2017
22	An Optimized Implementation Of IEEE-754 Floating Point Multiplier For DSP Applications	2017
23	Efficient Architecture For Processing Of Two Independent Data Streams Using Radix-2 FFT	2017
24	Implementation & Design Of Low Power Multiplier Using Fixed Width Replica Redundancy Block	2017
25	High Throughput DA-Based Fir Filter For FPGA Implementation	2017
26	Low Power And Area Efficient Wallace Tree Multiplier Using Carry Select Adder With Binary To Excess-1 Converter	2016
27	VLSI Design Of High Speed Vedic Multiplier For FPGA Implementation	2016
28	A Review On Power Optimized TPG Using LP-LFSR For Low Power BIST	2016
29	FPGA Based Hardware Implementation Of AES Rijndael Algorithm For Encryption And Decryption	2016
30	A Modified Partial Product Generator For Redundant Binary Multipliers	2016
31	Pipeline And Parallel Processor Architecture For Fast Computation Of 3D-DWT Using Modified Lifting Scheme	2016
32	Hybrid LUT/Multiplexer FPGA Logic Architectures	2016
33	Multi-Bit Flip-Flop Generation Considering Multicorner Multi-Mode Timing Constraint	2016
34	Carry Speculative Adder With Variable Latency For Low Power VLSI	2016

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35	A Synergetic Use Of Bloom Filters For Error Detection And Correction	2015
36	Fault Tolerant Parallel Filters Based On Error Correction Codes	2015
37	Obfuscating DSP Circuits Via High-Level Transformations	2015
38	A Generalized Algorithm And Reconfigurable Architecture For Efficient And Scalable Orthogonal Approximation Of DCT	2015
39	Scan Test Bandwidth Management For Ultra large-Scale System-On-Chip Architectures	2015
40	Fully Reused VLSI Architecture Of Fm0/Manchester Encoding Using Sols Technique For DSRC Applications	2015
41	Low-Power And Area-Efficient Shift Register Using Pulsed Latches	2015
42	High-Throughput Finite Field Multipliers Using Redundant Basis For FPGA And ASIC Implementations	2015
43	An Efficient Constant Multiplier Architecture Based On Vertical-Horizontal Binary Common Sub-Expression Elimination Algorithm For Reconfigurable FIR Filter Synthesis	2015
44	Low Delay Single Symbol Error Correction Codes Based On Reed Solomon Codes	2015
45	High-Throughput Finite Field Multipliers Using Redundant Basis For FPGA And ASIC Implementations	2015
46	Recursive Approach To The Design of a Parallel Self-Timed Adder	2015
47	Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic	2015
48	A Low Complexity Scaling Method For The Lanczos Kernel In Fixed-Point Arithmetic	2015
49	Design & Analysis of 16 bit RISC Processor Using low Power Pipelining	2015
50	Novel Block-Formulation and Area-Delay-Efficient Reconfigurable	2015

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	Interpolation Filter Architecture for Multi-Standard SDR Applications	
	BACK END DESIGN	
51	A Novel Five-input Multiple-function QCA Threshold Gate	2018
52	High speed and low power preset-able modified TSPC D flip-flop design and performance comparison with TSPC D flip-flop	2018
53	A New VLSI Architecture Of Power Efficient Nonvolatile Lookup Table Design Based On RRAM	2017
54	Low Power Area Efficient ALU With A Novel Full Adder	2016
55	Mixing Drivers In Clock-Tree For Power Supply Noise Reduction	2015
56	A Closed-Loop Reconfigurable Switched-Capacitor DC-DC Converter For Sub-Mw Energy Harvesting Applications	2015
57	Algorithm And Architecture For A Low-Power Content-Addressable Memory Based On Sparse Clustered Networks	2015
58	Statistical Analysis Of MUX-Based Physical Unclonable Functions	2015
59	Analysis And Design Of A Low-Voltage Low-Power Double-Tail Comparator	2015
60	Digitally Controlled Pulse Width Modulator For On-Chip Power Management	2015
61	A Multiobjective Optimization Based Fast And Robust Design Methodology For Low Power And Low Phase Noise Current Starved VCO	2015
62	Area Efficient Rom-Embedded SRAM Cache	2015